NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL
राष्ट्रीय प्रौद्योगिकी संस्थान कर्नाटक, सुरत्कल
P.O SRINIVASNAGAR, MANGALORE - 575025

IRIS

EC Call Letter List

M Tech. (Research), 2024 - 25

The following applicants have been selected for written exam and/or interview for the department for the department of Electronics and Communication Engineering for M Tech. (Research) Programme. The applicants are requested to go through additional information provided in their Call letters.

#	Name	Reference Number	Branch/Specialisation
1	TEEDA HEMANTH KUMAR	MTR2024VL0001	VLSI Design
2	MUPPALLA NITHEESH KUMAR	MTR2024VL0004	VLSI Design
3	Rahul Babu Thorat	MTR2024VL0005	VLSI Design
4	HAMAD KHALID BAIG	MTR2024VL0006	VLSI Design
5	HAMAD KHALID BAIG	MTR2024SP0001	Signal Processing and Machine Learning
6	Ankit kumar	MTR2024VL0007	VLSI Design
7	Prabhas K Deshpande	MTR2024VL0008	VLSI Design
8	SOUMALYA BISWAS	MTR2024VL0009	VLSI Design
9	MANOJ KUMAR CM	MTR2024VL0011	VLSI Design
10	ANJALI L	MTR2024VL0012	VLSI Design
11	BISHAL BHATTACHARJEE	MTR2024VL0013	VLSI Design
12	Sahana C	MTR2024CN0002	Communication Engineering and Network
13	Greeshma Varma	MTR2024VL0014	VLSI Design
14	Vaibhav Singh	MTR2024VL0015	VLSI Design
15	SHEIKH MUJAHID UL ISLAM HAMZA	MTR2024VL0016	VLSI Design
16	VARUN KUMAR	MTR2024VL0017	VLSI Design
17	Naveen	MTR2024SP0006	Signal Processing and Machine

प्राध्यापक एवं विभागाध्यक्ष/ PROF & HEAD
इ. एवं सी. विभाग / Department of E & C
एन.आई.टी.के. सुरत्कल/NITK Surathkal
मंगलूरु / MANGALURU - 575 025

IRIS

EC Call Letter List

M Tech. (Research), 2024 - 25

#	Name	Reference Number	Branch/Specialisation
18	RAJESH THAKUR	MTR2024SP0007	Signal Processing and Machine Learning
19	VISHNU N	MTR2024SP0008	Signal Processing and Machine Learning
20	POOJA P	MTR2024VL0023	VLSI Design
21	POOJA P	MTR2024CN0004	Communication Engineering and Network
22	Robin Roy	MTR2024VL0025	VLSI Design
23	Adarsh Pandey	MTS2024VL0026	VLSI Design
24	Konduri Hemant Sastry	MTR2024SP0010	Signal Processing and Machine Learning
25	Bhanse Jayant Zunjar	MTR2024VL0027	VLSI Design
26	Bhanse Jayant Zunjar	MTR2024SP0011	Signal Processing and Machine Learning
27	Shubham Chandra	MTR2024VL0028	VLSI Design
28	Girish Babu B	MTR2024VL0029	VLSI Design
29	JATIN	MTR2024VL0030	VLSI Design
30	Tauseef khan	MTR2024VL0032	VLSI Design
31	RAJEEV RANJAN	MTR2024VL0034	VLSI Design

Head Of Department
Electronics and Communication Engineering

प्रोफेसर एवं विभागाध्यक्ष/PROF & HEAD
इ. एवं सी. विभाग / Department of E & C
एन.आई.टी.के. सुरत्कल/NITK Surathkal
मंगलूर / MANGALURU - 575 025

Dean Academics

NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL
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IRIS

EC Call Letter List

M Tech (Sponsored), 2024 - 25

The following applicants have been selected for written exam and/or interview for the department for the department of Electronics and Communication Engineering for M Tech (Sponsored) Programme. The applicants are requested to go through additional information provided in their Call letters.

#	Name	Reference Number	Branch/Specialisation
1	ALLU ASHOK KUMAR	MT2024EC0001	Electronics and Communication Engineering
2	AKHILA S KOUSHIK	MT2024EC0002	Electronics and Communication Engineering

Head Of Department
Electronics and Communication Engineering

PROF & HEAD
Dept. of E&C
एन.आई.टी.के. सुरत्कल/NITK Surathkal
मंगलूर / MANGALURU - 575 025

Dean Academics

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA SURATHKAL
P.O. SRINIVASNAGAR, MANGALURU-575 025
Telephone: 0824-2473046, Website: www.ece.nitk.ac.in

Date: 03-05-2024

Shortlisted candidates for M Tech (R/S) Programme–Written Aptitude Test / Interview for the year 2024-25

With reference to your application for admission to M Tech (R/S) Programme in the department of Electronics and Communication Engineering, you are requested to appear for the Written test/Interview at NITK Surathkal. You should produce all the original records such as Date of Birth Certificate, GATE Score Card, Degree Certificate and Marks Cards of all semesters (UG programme), SC/ST/OBC/EWS certificate (if applicable as per proforma), Person with disability certificate (if applicable), Sponsorship letter (if applicable), Conduct Certificate and valid photo identity card. Please keep a self-attested photocopy of all these certificates readily available at the time of interview.

Department	: Department of Electronics and Communication Engineering
Place of Reporting	: Department of Electronics and Communication Engineering, NITK Surathkal
Written Test Date and Time	: May 15, 2024, 9.00 AM at ECE Department
Announcement of shortlisted candidates for interview	: May 15, 2024, 12.00 PM
Interview Date and Time	: May 15, 2024, 2.00 PM Onwards, Meeting room, ECE Department

NOTE:

1. Candidates should be prepared to appear for a written Aptitude Test before the interview.
2. Fee Structure for M Tech (S/R) programme and Course syllabus are provided on Institute's website, i.e. www.nitk.ac.in. A copy of the syllabus for the aptitude test is given in a separate page.
3. Full-time/External Registrants - sponsored from Industry or other organizations, should have been serving in the sponsoring organisation for a period of **at least 2 years** after qualifying degree and have to produce a letter from their employer stating that the candidate is deputed for M Tech / M Tech (Research) in the Institute on full salary during the study period. The employer should indicate that the candidate will not be withdrawn midway before the completion of the course. (Sponsorship letter should be in the format provided in the Application Form).
4. Candidates who have not submitted marks of final examination along with application form shall produce the same at the time of admission if available.
5. Your candidature for this test is provisional & is subject to your fulfilling the educational qualifications & other criteria prescribed for the programme as mentioned in the Information Brochure, failing which your candidature can be summarily rejected after verification/scrutiny at a later stage.
6. Please keep the Admit Card ready during the offline test and interview. You are responsible for safe custody of the Admit Card and in the event of any other person using this Admit Card, the responsibility lies on you to prove that you have not used the service of an impersonator.
7. Please note that no expenses shall be payable for appearing in the written test/Interview.

Head of the Department

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Date: 03-05-2024

Syllabus for M. Tech. (Research) Aptitude Test- May 2024

The Test paper has 2 Parts, Part-1 is compulsory, and Part-2 is stream specific modules. The candidate is supposed to attempt Module A or Module B or Module C from Part-2 depending on the candidature for a particular M. Tech(R) streams. Part-1 has 15 multiple choice type questions, whereas, each module of Part-2 has 15 multiple choice type questions. Each correct answer carries 1 mark and wrong answer carries -0.25 marks.

Note: Total duration of Exam is one hour. Calculator is permitted.

Part-1:

Linear Algebra, Calculus, Differential and Difference equations. Numerical methods, Transforms, Linear circuits and networks, Electronic components and Devices, Analog Electronics, Digital Electronics, Signals and Systems, Linear and Digital Control Theory.

Part-2:

Module-A (CEN Stream)

Electromagnetic Waves, Probability and Random Processes, Communication Theory, Communication Circuits, Transmission Lines, Wave Guides, Antennas, Microwave devices and Circuits, Data Communications, Communication Networks, Satellite Communication, Optical Communication, Fundamentals of Signal Processing.

Module-B (SPML stream)

SP Fundamentals: Time domain analysis of discrete-time systems - Basic discrete time signals, discrete-time Fourier Series, Z Transform – definition and properties, Discrete-time Fourier Series and its properties, Properties and applications of DTFT. Relationship between time, Z and frequency domains, DFT fundamentals and Properties of DFT, FIR and IIR filters.

Data Structure Fundamentals: Algorithm analysis, Asymptotic notations. Divide and Conquer algorithms, Analysis of divide and conquer algorithms, master method, examples - merge sort, quick sort, binary search, Data structures, Linked list, stacks and queues.

Module-C (VLSI Design)

Linear and Digital ICs, Digital System Design, VLSI Technology, CMOS VLSI, Mixed Signal Design, HDL, Data converters, Microprocessors, Computer Architecture and organization, Logic Synthesis, DSP Architectures, Embedded Systems.